

Serial No. 09/614,113

IN THE CLAIMS:

It is proposed that claims 6 and 7 be amended as hereinafter set forth and that claims 1 through 5 and 8 through 16 be canceled without prejudice or disclaimer. Upon entry of the proposed amendments and cancellations, this listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

Claims 1 and 2 (Previously Withdrawn and Canceled Herein)

Claims 3 through 5 (Canceled)

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Claim 3 (Amended): ~~The method of claim 3,~~ A method of forming a gate stack,
comprising:

forming a gate dielectric layer on a silicon substrate;
forming a polysilicon layer on top of the gate dielectric layer;
subjecting the polysilicon layer to an ion implantation of impurities;
depositing a metallic silicide film in a non-annealed state atop the polysilicon layer; and
depositing a dielectric cap layer over the metallic silicide film at a temperature below
about 600°C., wherein said depositing a dielectric cap layer over said metallic silicide film is
effected at a the temperature is sufficiently low to maintain said the metallic silicide film in said
the non-annealed state.

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Claim 4 (Amended): ~~The method of claim 3,~~ A method of forming a gate stack,
comprising:

forming a gate dielectric layer on a silicon substrate;
forming a polysilicon layer on top of the gate dielectric layer;
subjecting the polysilicon layer to an ion implantation of impurities;
depositing a metallic silicide film in a non-annealed state atop the polysilicon layer; and

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depositing a dielectric cap layer over the metallic silicide film at a temperature below about 600°C, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature is sufficiently low to preclude formation of silicon clusters in said the metallic silicide film.

Claims 8 through 16 (Canceled)

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Claim 11 (Original): A method for forming a gate stack, comprising:
providing a semiconductor substrate with a dielectric layer on an active surface of said semiconductor substrate, wherein a polysilicon layer is disposed over said dielectric layer;
forming a metallic silicide film in a non-annealed state over said polysilicon layer;
forming a dielectric cap on said metallic silicide film at a sufficiently low temperature that said metallic silicide film remains in said non-annealed state;
forming and patterning a resist layer on said dielectric cap;
etching said dielectric cap, said metallic silicide film, and said polysilicon layer; and
stripping said resist layer.

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Claim 12 (Original): The method of claim 11, wherein forming said dielectric cap is effected at a temperature below about 600° C.

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Claim 19 (Previously Added): A method of forming a gate stack, consisting essentially of:
forming a gate dielectric layer on a silicon substrate;
forming a polysilicon layer on top of the gate dielectric layer;
subjecting said polysilicon layer to an ion implantation of impurities;
depositing a metallic silicide film in a non-annealed state atop said polysilicon layer; and
depositing a dielectric cap layer over said metallic silicide film at a temperature below about 600 °C such that the metallic silicide film remains in said non-annealed state.

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Claim ~~20~~ (Previously Added): The method of claim ~~19~~, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature of between 400°C and 600°C.

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Claim ~~21~~ (Previously Added): The method of claim ~~19~~, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature of about 500°C.

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Claim ~~22~~ (Previously Added): The method of claim ~~19~~, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature sufficiently low to preclude formation of silicon clusters in said metallic silicide film.